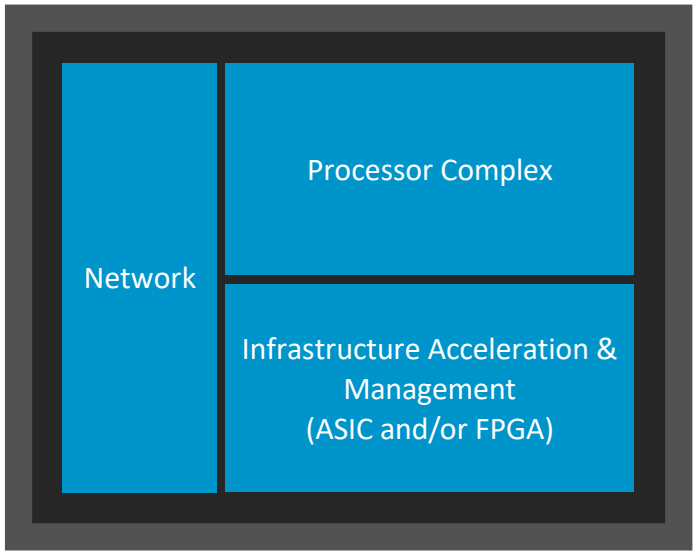

June 13-15, 2023
DoubleTree by Hilton San Jose
SmartNICsSummit.com

# High-Speed Secure Virtual Application Delivery Using FPGA-Based SmartNICs

Presented by Geetha Jayagopi and Tim Michels

# Intel® Infrastructure Processing Unit (IPU)

## Providing new data center value



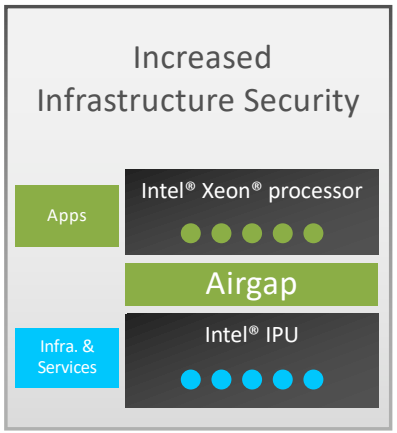

- Highly intelligent infrastructure acceleration
- System-level security, control, and isolation
- Common software frameworks
- HW and SW programmable, built to customer needs

intel.com/ipu

*Processor complex enables control plane offload and isolation*

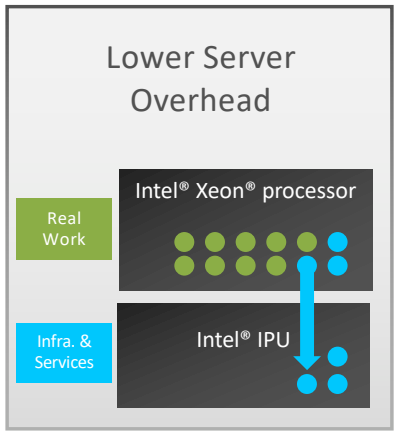
# Intel® IPU Value Proposition

## Security



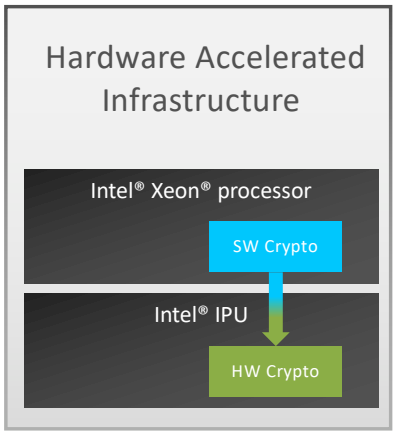

Application & Tenant Isolation from Infrastructure

## Infrastructure Offload



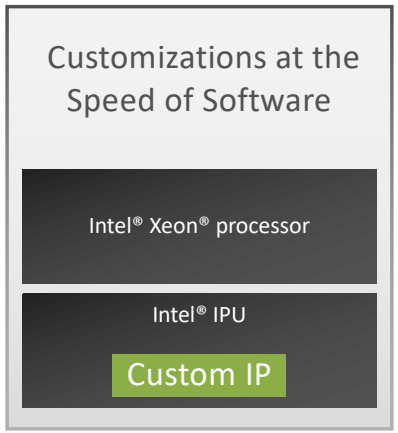

IPUs Reduce Host Compute Cycles Doing Infrastructure Work

## Infrastructure Acceleration




IPUs Can Accelerate Some Applications

## Feature Velocity




IPUs Provide Reconfigurability and Programmability

*Isolation of workload and infrastructure improves integrity and efficiency of the grid*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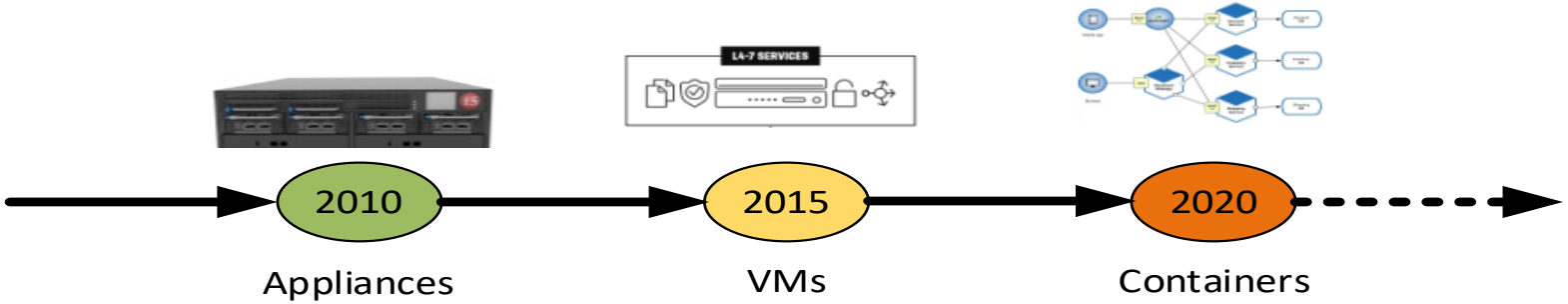
# Accelerating Application Services

Tim Michels
Distinguished Engineer, F5 Inc

# F5 is a Leading ADC Systems Company

- Custom built BIG IP appliances and Chassis
- Integrated CPU's, ASICs, and FPGAs
- Hardware acceleration
  - Flow Aware
  - Packet Transforms
  - PKI and Bulk Cryptography
  - DDOS Filters

# But F5 Product Deployments have Evolved….



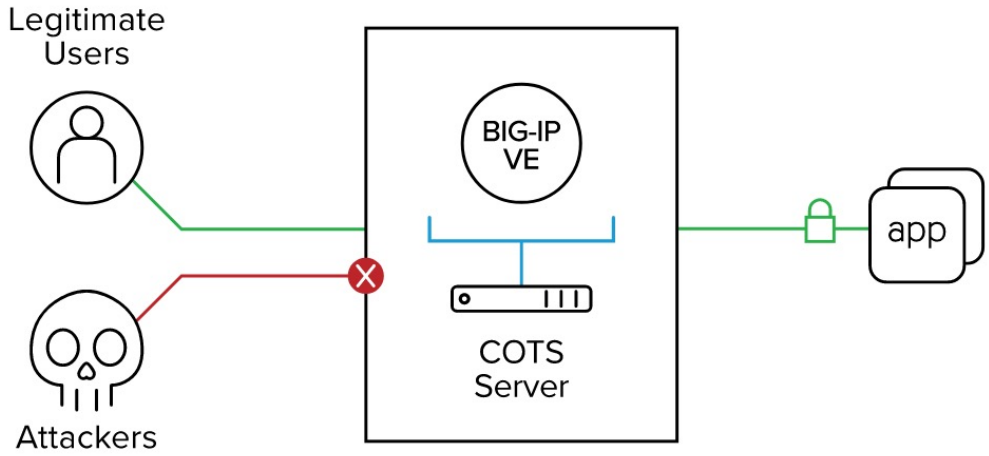

## Appliances

- Traditional 3-Tier architecture friendly
- Scale up capacity with hardware accelerators
- Difficult to integrate with Cloud architectures

## Virtualized Services

- VMs initially and now Containers and Micro-services
- Scale out capacity by clustering many instances
- Easily integrated in cloud deployments
- But there is a problem…..!!!

# The Single Node Bottle Neck

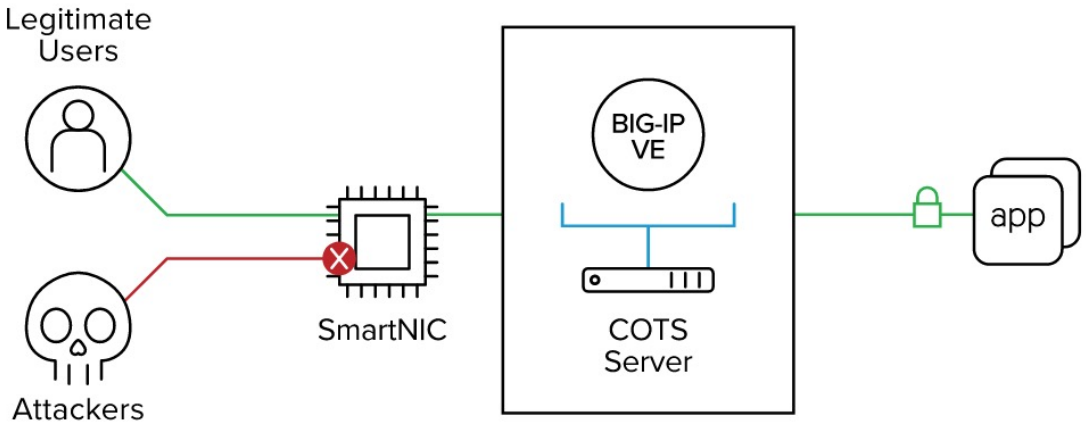



Single node performance matters!

Common Occurrences

- Session or Subscriber State Pinning
- Security Policy Chokepoints
- DoS attack against scale out algorithm

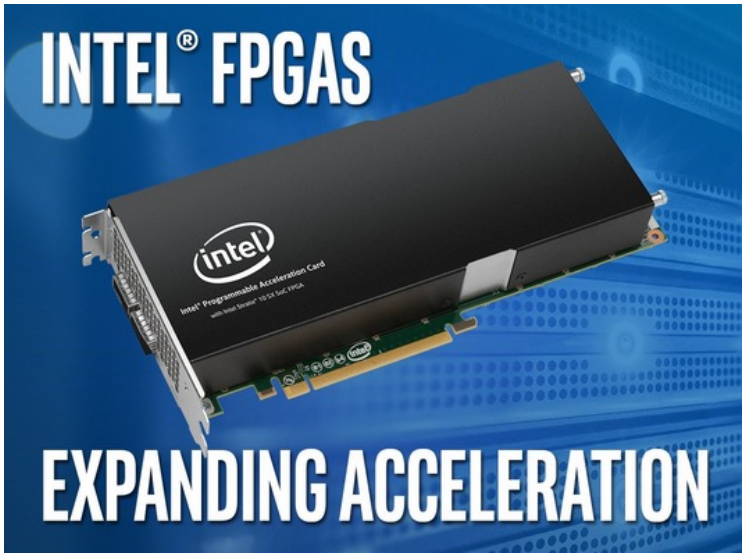
# The Single Node Bottle Neck – Fixed!




- Single node performance matters!
- Common Occurrences
  - Session or Subscriber State Pinning
  - Security Policy Chokepoints
  - DoS attack against scale out algorithm
- **Hardware acceleration in the node is the answer**

# Why F5 Chose an FPGA SmartNIC?

- F5's Acceleration History
  - Existing IP Library
  - Easy lift for F5 software
- FPGA cards are a natural fit
  - PCIe and Ethernet in the right layout
  - External memory support
- Very Capable
  - High density and high-performance logic
  - Familiarity with tooling and devices



# Example: DDOS Protection

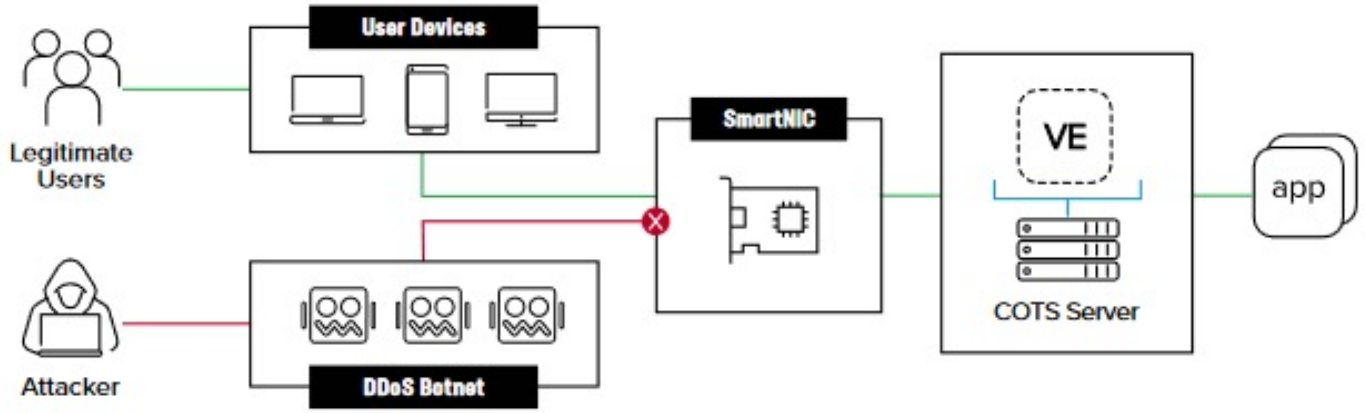
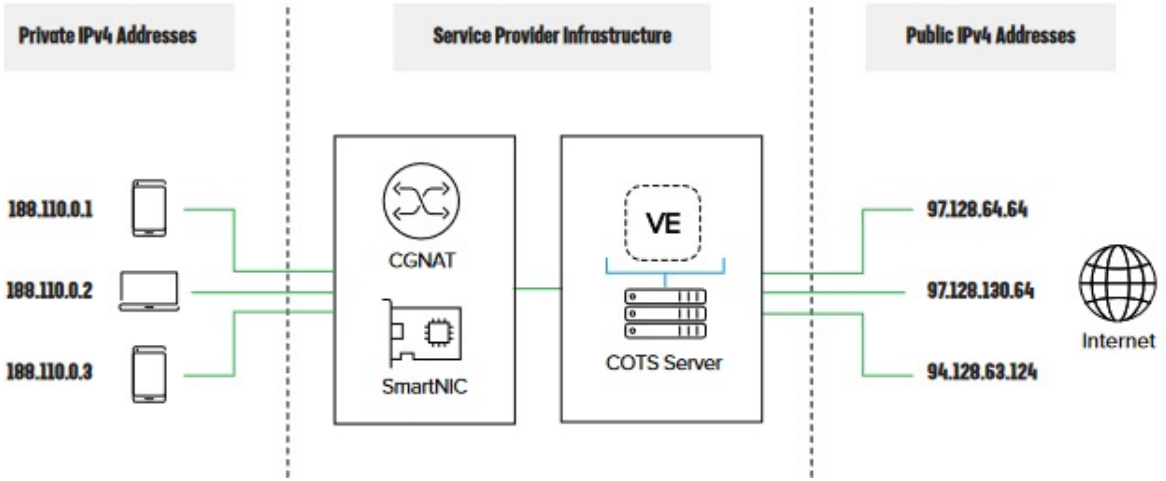



**Table 3:** Performance data for the BIG-IP VE and BIG-IP VE for SmartNICs solution when mitigating a combined SYN-ACK flood, UDP flood, and ICMPv4 flood DDoS attack.

| | Max. Withstandable Attack Size | VE CPU Utilization |
|---|---|---|
| BIG-IP VE | 2.4 Gbps | 100% |
| BIG-IP VE for SmartNICs | 40 Gbps | 29.8% |

# Example: Carrier Grade NAT




**CGNAT Performance Comparison**

| | L4 Throughput | VE CPU Utilization |
|---|---|---|
| BIG-IP VE | 37 Gbps | 87% |
| BIG-IP VE for SmartNICs | 48 Gbps | 4% |

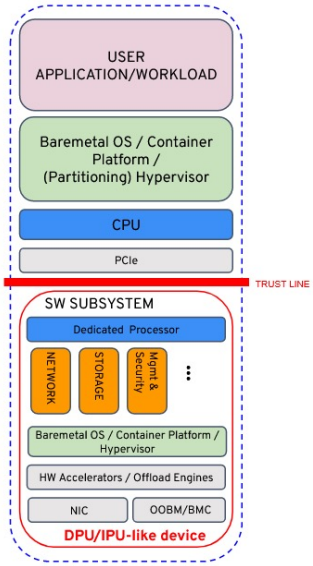
**Table 1:** Performance comparison for the BIG-IP VE for SmartNICs solution when operating NAT44 in NAPT mode

# BIG IP VE with SmartNIC

N5013 (100Gbps TP w/ 2x100GE ports)

https://www.f5.com/pdf/solution-overview/augment-performance-virtualized-environments-with-big-ip-ve-for-smart-nics.pdf

# Acceleration Futures



Physical server

## IPU Enabled Architectures

- Move F5 software onto the IPU card
- Whole cloth infrastructure services on card
- Powerful model for Edge  and Service Provider use cases
- F5 is active in the Open Programable Infrastructure (OPI) project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# Thank You