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THE RISC-V PERFORMANCE LEADER

RISC-V + Chiplet to Enable Full Stack Acceleration for the Datacenter

Ventana: High Performance RISC-V + Chiplet Leader

Balaji Baktha
Founder and CEO

Pioneer in Data Center semiconductors: 30+ years experience

- World's first 64-bit ARM with Veloce (Acquired by AppliedMicro)
- Led Marvell BU delivering Data Center class Networking, Communications, Compute, Storage and Wireless infrastructure products
- World's first iSCSI with Platys, acquired by PMC-Sierra (Adaptec)

Greg Favor
Co-founder and Chief Architect

One of the world's leading CPU architects: 35+ years experience

- Architected K6 processor at startup Nexgen, acquired by AMD
- Chief Architect at Siara Systems, acquired by RedBack
- Architected first successful 64-bit ARM CPU

Founded in 2019 by industry veterans with a proven track record of delivering Data Center class processors

- Highly experienced team with over 20 years average experience
- Core team developed world's first 64-bit High Performance ARM Processor (Veloce Technologies)
- Delivered several successful x86 processors with AMD
- Software team that enabled ARM for data center now doing RISC-V

Ventana Confidential

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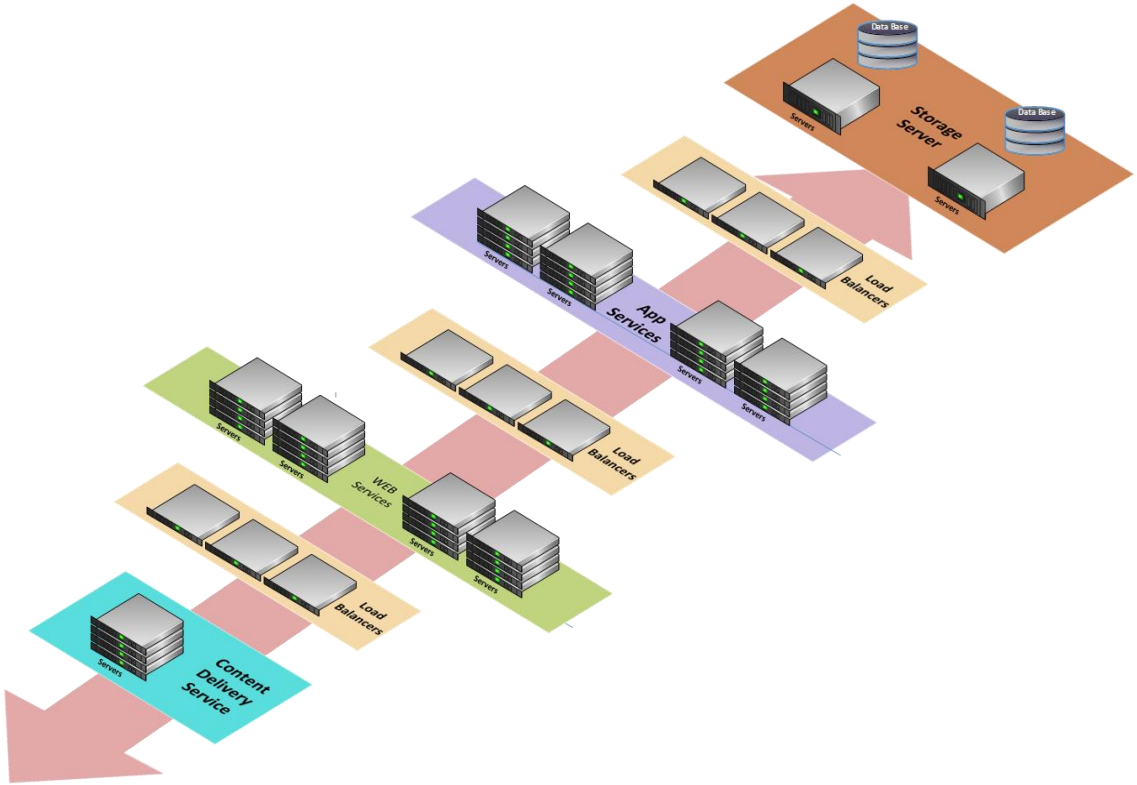
Typical Datacenter Architecture

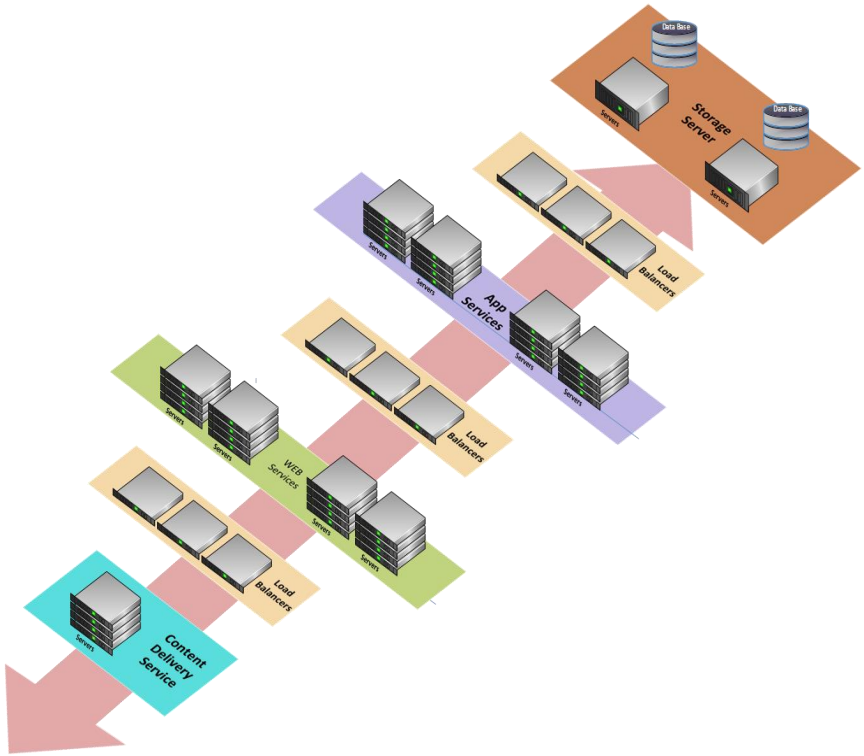


- Storage Servers
- Load Balancers
- App Services
- Load Balancers
- Web Services
- Load Balancers
- Content Delivery Services

Networking Services

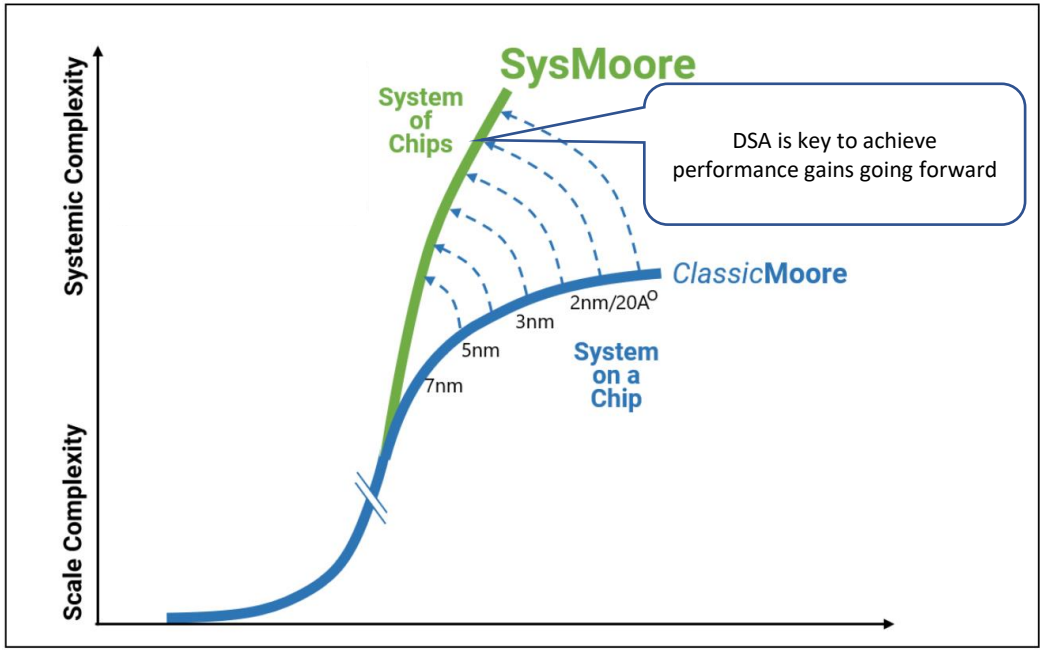
Application Compute is ~60%, Infrastructure Compute is ~40%

Accelerator Use Cases



Workloads	Accelerators
Databases Redis, MySQL	Key/Value Acceleration
Computational Storage CEPH	Compression/Encryption
Data Analytics, Search SPARK, Elastic Search, Solr	Algorithmic Acceleration
AI/ML TensorFlow, PyTorch	Training, Inference
Web Services Apache, Memcached	Web Serving, Caching
CDN Mediawiki, Streaming	Transcoding
Networking/ Infrastructure Offloads	Packet Parsing, Classification, TCP Offload, RegEx

Domain Specific Acceleration for Workload Efficiency

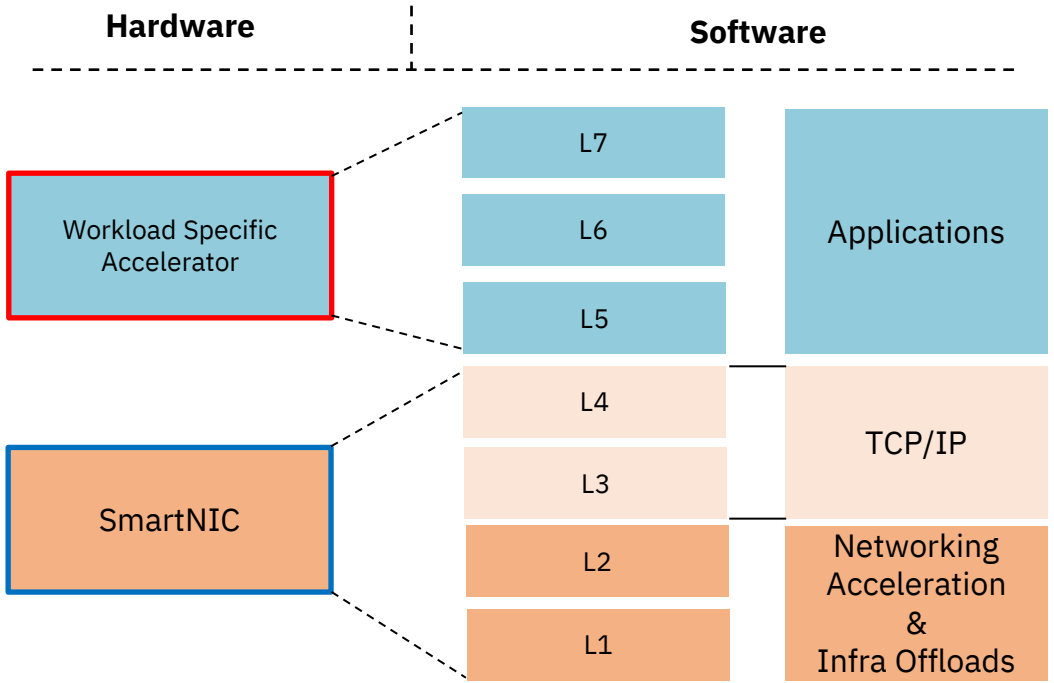


Source: Synopsys, https://www.synopsys.com/glossary/what-is-sysmoore.html

- Full stack acceleration is key to achieve best in class performance
- SmartNIC + DSA

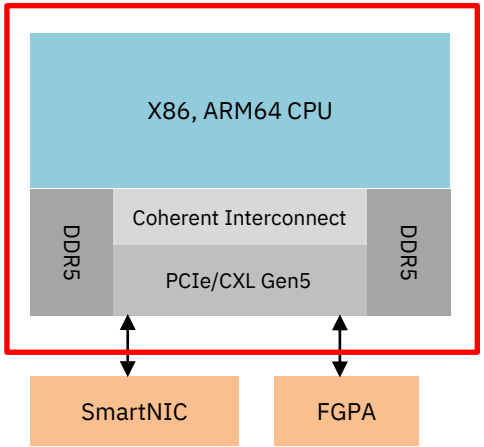
Full Stack Acceleration Overview

- **SmartNIC**
  - Network Acceleration
  - Datapath Processing Acceleration
  - Infrastructure Offloads
- **Workload Accelerator (DSA)**
  - Adds workload specific acceleration
  - Web Services, Databases, Storage, Security, AI/ML



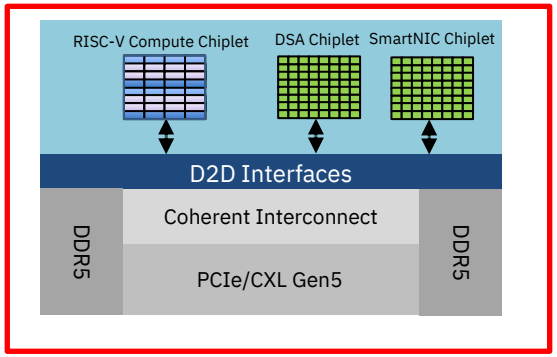
Next Gen Accelerator Architecture with RISC-V and Chiplets

Traditional SmartNICs



- Multiple memory copies lower performance and increases power
- High latency PCIe interface
- Limited programmability – fixed function acceleration

Chiplet based Domain Specific Accelerator



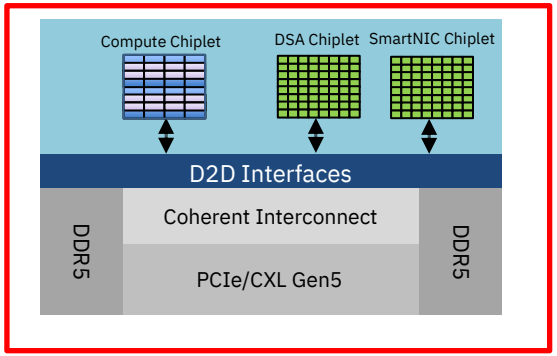
- RISC-V's ISA extensibility is a key enabler
- Scalable Compute, Accelerator and I/O performance
- Low latency, low power parallel D2D interface
- Coherent memory eliminates data copies, improves performance
- Fully programmable, flexible architecture

DSA Building Blocks

Hardware/Software Codesign

- RISC-V ISA Extensions and Custom Instructions
- Domain Specific Accelerators
- Infrastructure Offloads
- Full Software Programmability
- Simple Programming Model
  - Same programming model for host and DSA
- Unified Compiler

Chiplet based Domain Specific Accelerator



In Closing …

- RISC-V ISA's extensible architecture, and Chiplets are needed to drive overall efficiency for full stack acceleration in the datacenter
- Ventana leads the market with the RISC-V based Veyron CPU cores and chiplets
- Ventana is uniquely positioned to drive the datacenter accelerator segment

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Thank You