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Session A-103: Network Acceleration 2

Removing the Tail from SmartNIC Latency

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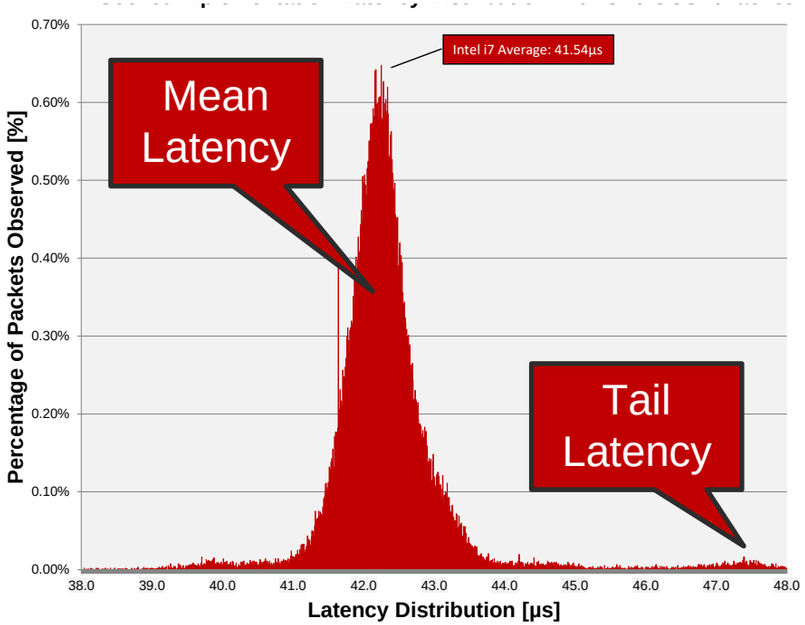
4:20pm

Perspectives

- **Tail Latency is a root of evil in Networks**
  - It delays application response time
    - When will this program complete?
  - It adds uncertainly to transactions
    - Has it completed yet?
  - It gets worse with more software
    - Layers on layers



Read Latency of a Key Value Store implemented in Software on a CPU

Multiple Sources Latency in Software-based NICs

- PCIe Bus Scheduling
- DMA Scatter/Gather
- DRAM Refresh
- Operating System Scheduler
- Software Libraries
- CPU Cache Miss

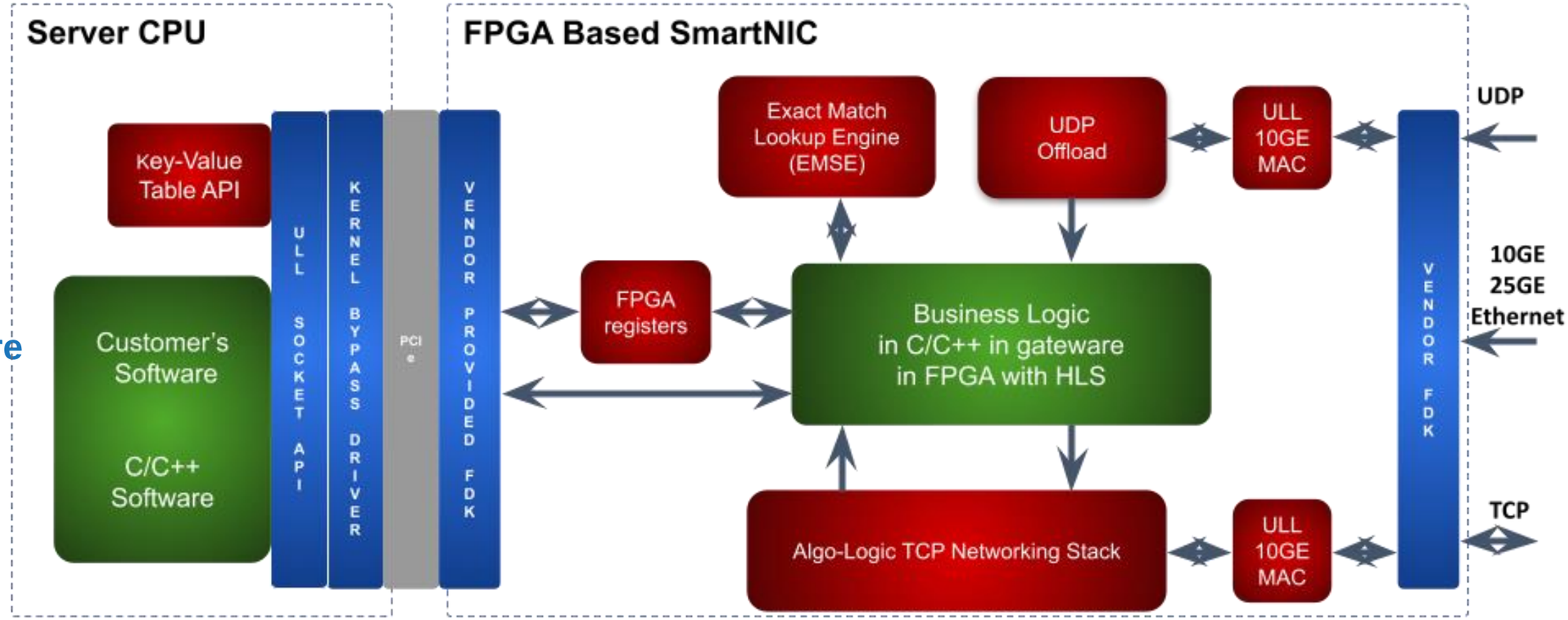
…

Ultra Low Latency Applications run well on FPGA SmartNICs

- **Tick-to-Trade**
  - Proprietary Traders demand sub-microsecond latency
  - Equities, Futures, and Options trade using UDP/IP and TCP/IP
  - High Frequency Trading systems source 70% of orders on modern exchanges
- **Pre-Trade Risk Checks**
  - Verify Compliance as orders flow through network
  - Requires full-stack processing with sub-microsecond Latency
- **Real-Time Data Processing**
  - Real-time sensors and actuators need deterministic response times
  - Key Value Store (KVS) provides associative Lookup in FPGA hardware
  - Entangled Applications

Ultra Low Latency (ULL) Framework for FPGA SmartNICs

- **Algo-Logic IP cores**
  - ULL MAC
  - UDP Offload
  - TCP Stack
  - Registers for API
- **FPGA Vendor Hardware**
  - Software Drivers
  - PCIe / CXL
  - Interface to SERDES
- **Customer**
  - Software
  - Business Logic
    - Coded in Verilog or with High Level Synthesis (HLS)

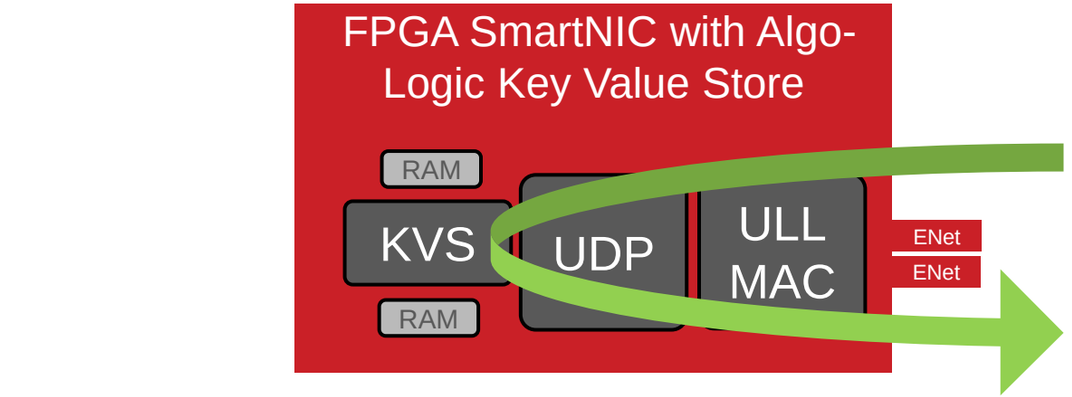


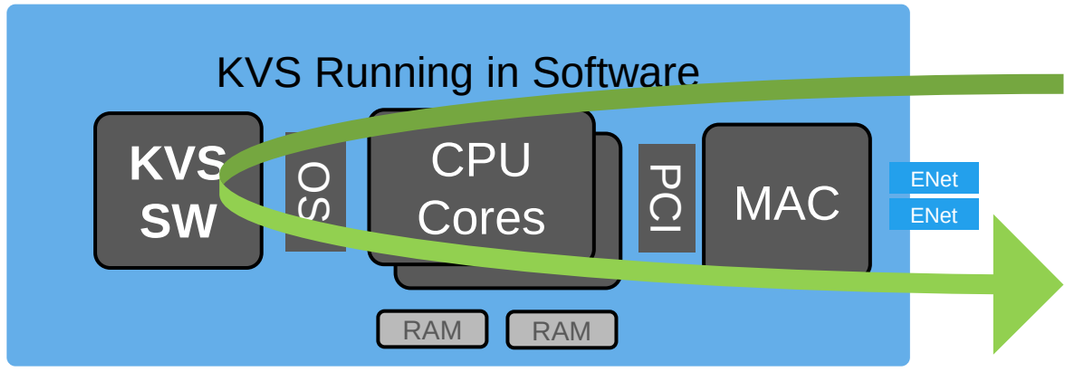
Algo-Logic IP Cores
FPGA Vendor Hardware + Software Driver
Customer Software and Business Logic

AMD cisco intel

Key Value Store implemented on FPGA SmartNIC vs Software

- **FPGA SmartNIC with KVS in FPGA**
  - **ULL PHY+MAC (ULL MAC)**
    - Ultra Low Latency Ethernet
  - **UDP/IP Endpoint (UDP)**
    - Terminates Layer 4 to logic
  - **Key Value Store (KVS)**
    - In Memory Associative Table
- **Software with KVS running on CPU Cores**
  - **Ethernet MAC**
  - **PCIe to CPU core**
  - **KVS running Software**
    - Operating System
    - Network stack In kernel
    - KVS Application in Software



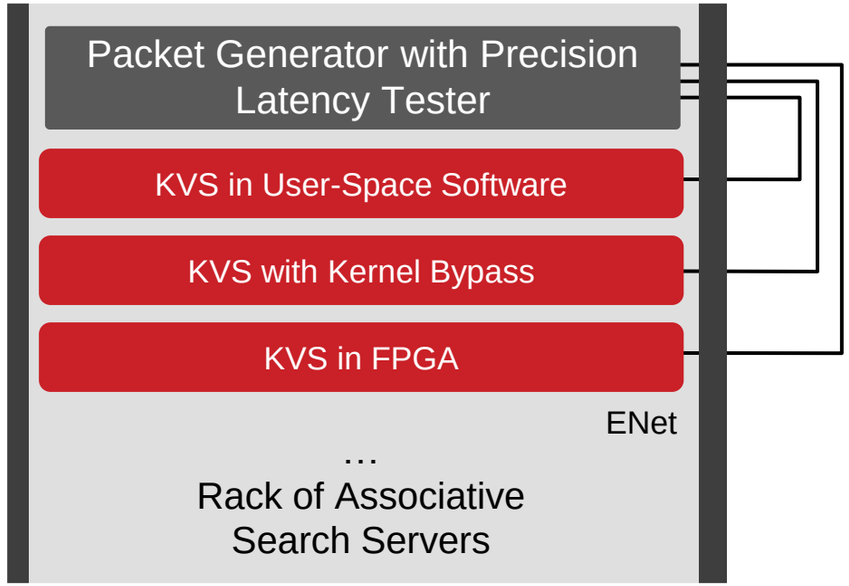


KVS Read:

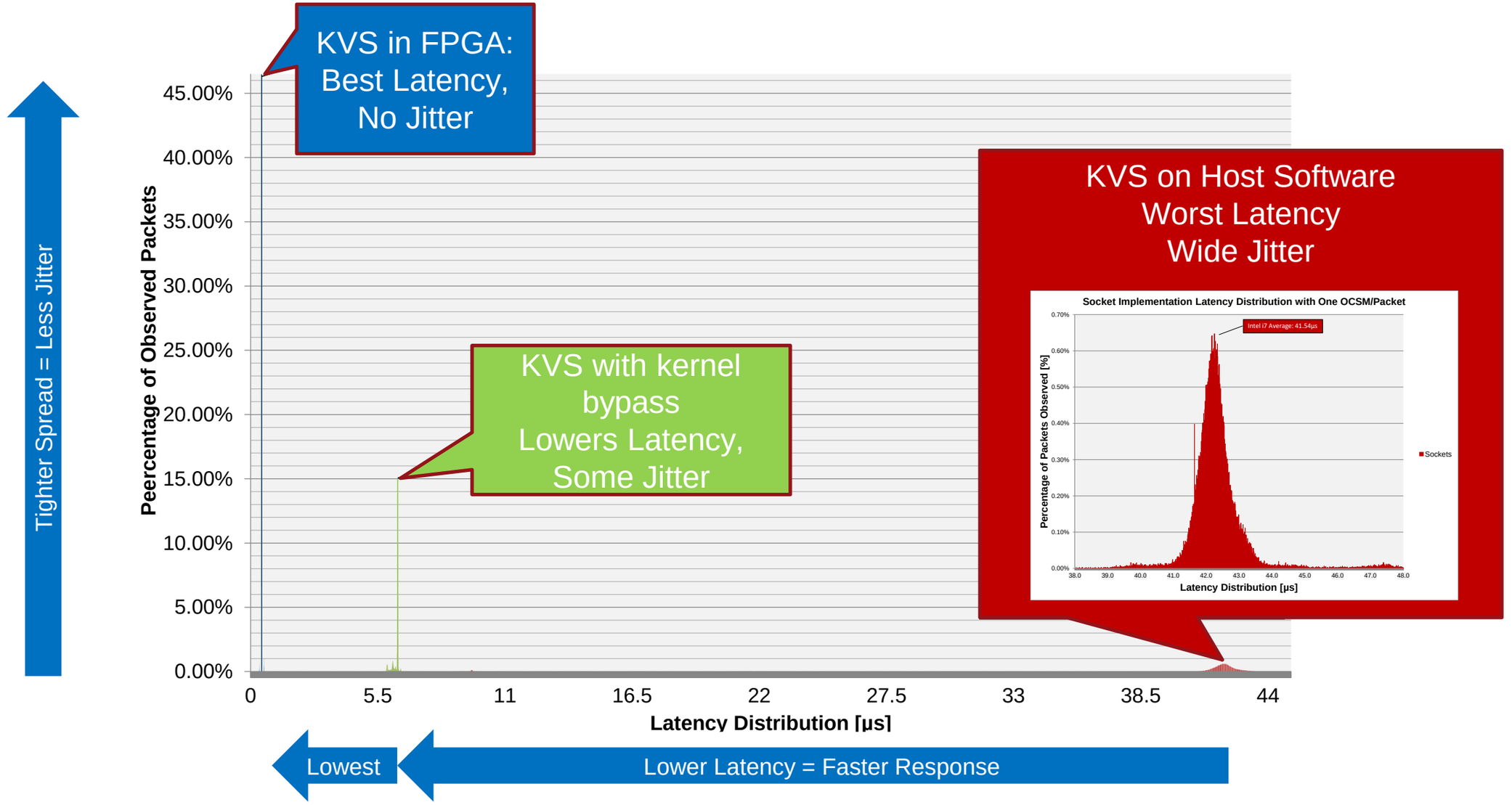
Latency, Measured externally from server

Measured Latency of FPGA SmartNIC

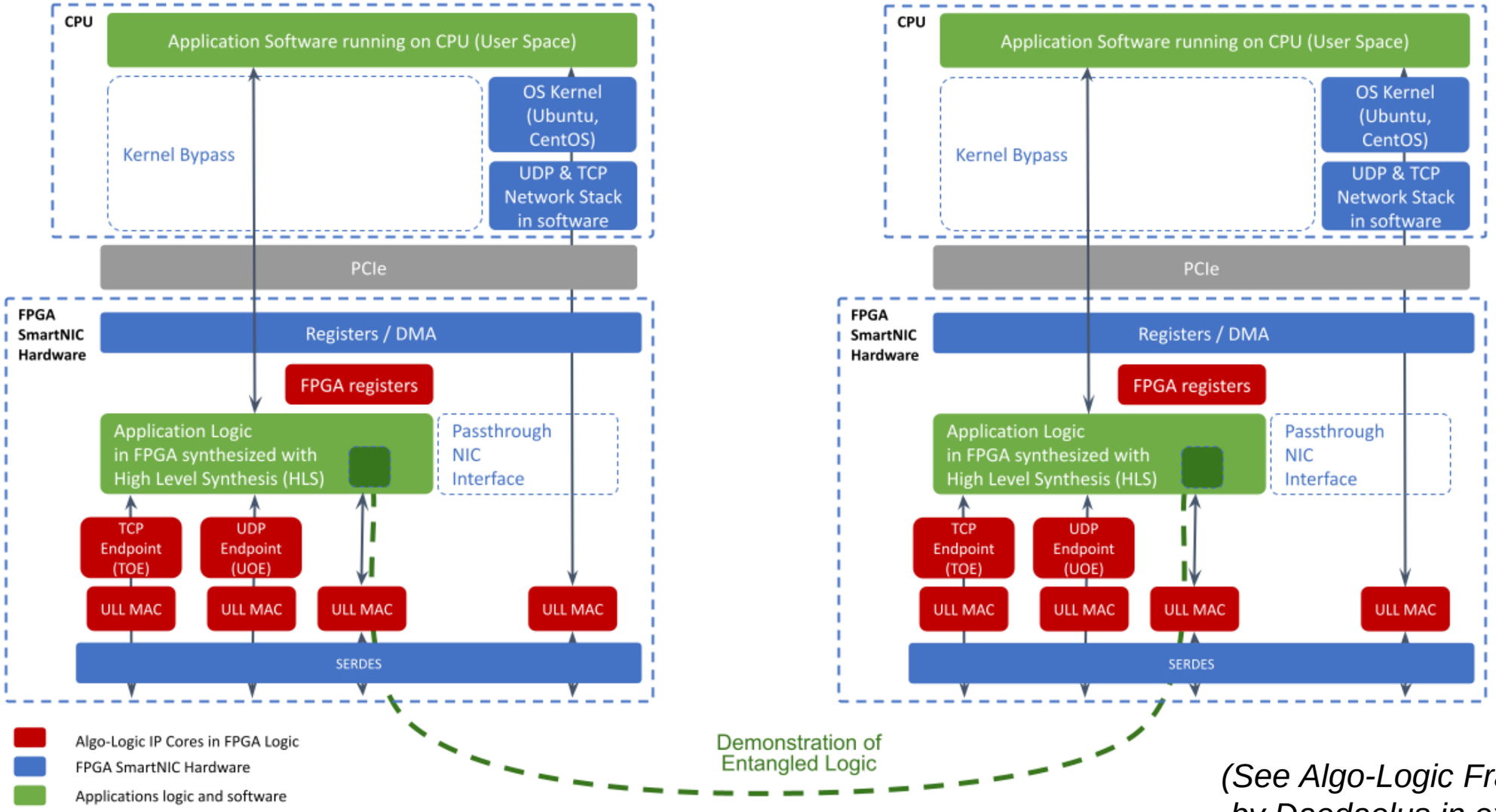
- **Packet Generator**
  - Sends packets to Key Value Stores over Ethernet
  - Requests contain keys to read values in packets
  - Precisely measures network response time
- **KVS in User Space Software**
  - X86 CPU (Core i7)
  - Linux Operating System (CentOS)
  - User Space Application
- **Kernel Bypass**
  - SmartNIC bypasses Operating System
  - Applications directly process incoming packets
- **KVS in FPGA**
  - Datapath implemented fully in Logic



KVS Latency in FPGA on SmartNIC vs Software on Host CPU



Demonstration of Entangled Application on FPGA SmartNIC



(See Algo-Logic Framework in use by Daedaelus in expo room)

Transactions Complete Faster when they run on Ultra Low Latency Framework

Conclusions

- **Algorithms implemented in Logic on SmartNICs are**
  - Flexible:
    - FPGA Logic optimized to match application
  - Deterministic:
    - Datapath has constant latency with no tails
  - Fast:
    - Ultra Low Latency with sub-microsecond full-stack response times
- **Many Applications benefit from ultra low latency**
  - Trading (HFT, Compliance)
  - Databases (Key Value Store)
  - Entangled Applications
- **Algo-Logic frameworks run on multiple platforms**