



**April 26-28, 2022**  
**DoubleTree by Hilton San Jose**  
**SmartNICsSummit.com**

# State of SmartNICs Today

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# Agenda

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- News
- Architectures
- Products
- Future Architectural Directions

## \$1.9 Billion for Pensando!

1. Clearly not revenue play, otherwise 40X multiplier?
2. Genius move by AMD, for many reasons:
  - a. Took Pensando off the board
  - b. Blocks Cisco from proven mass market SmartNIC
  - c. Clearly a move to dominate the data center
  - d. An AMAZING chiplet story?

Combine Xilinx FPGA, x86 cores and Pensando I/O

# New Perspective

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The Data Center is the New Computer

SmartNICs will be the Execution Platform  
for the Data Center OS

# Architectures & Products

- Architectures

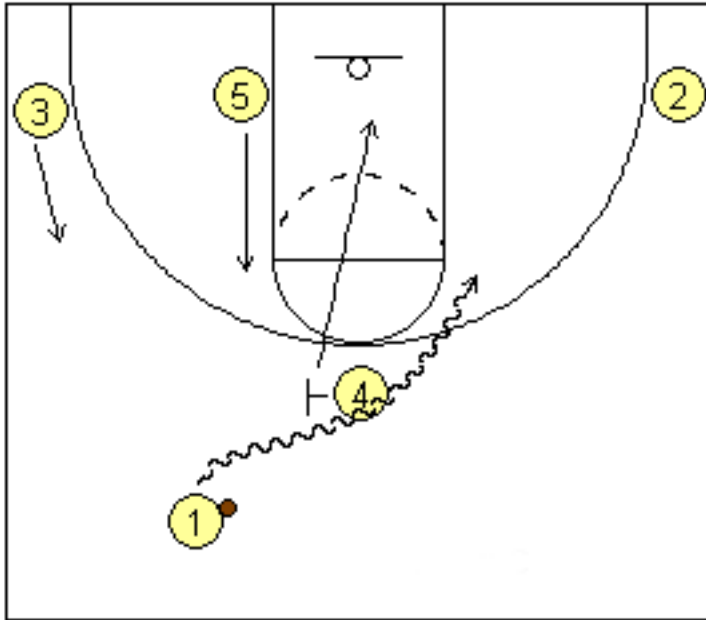
- Control vs. Data Plane
- Classic (Arms with IP & NoC)
- FPGA
- Hybrid (ASIC NIC / Arm / IP / x86)

- Products

- Intel, Marvell, Napatech, NVIDIA, Pensando, Xilinx



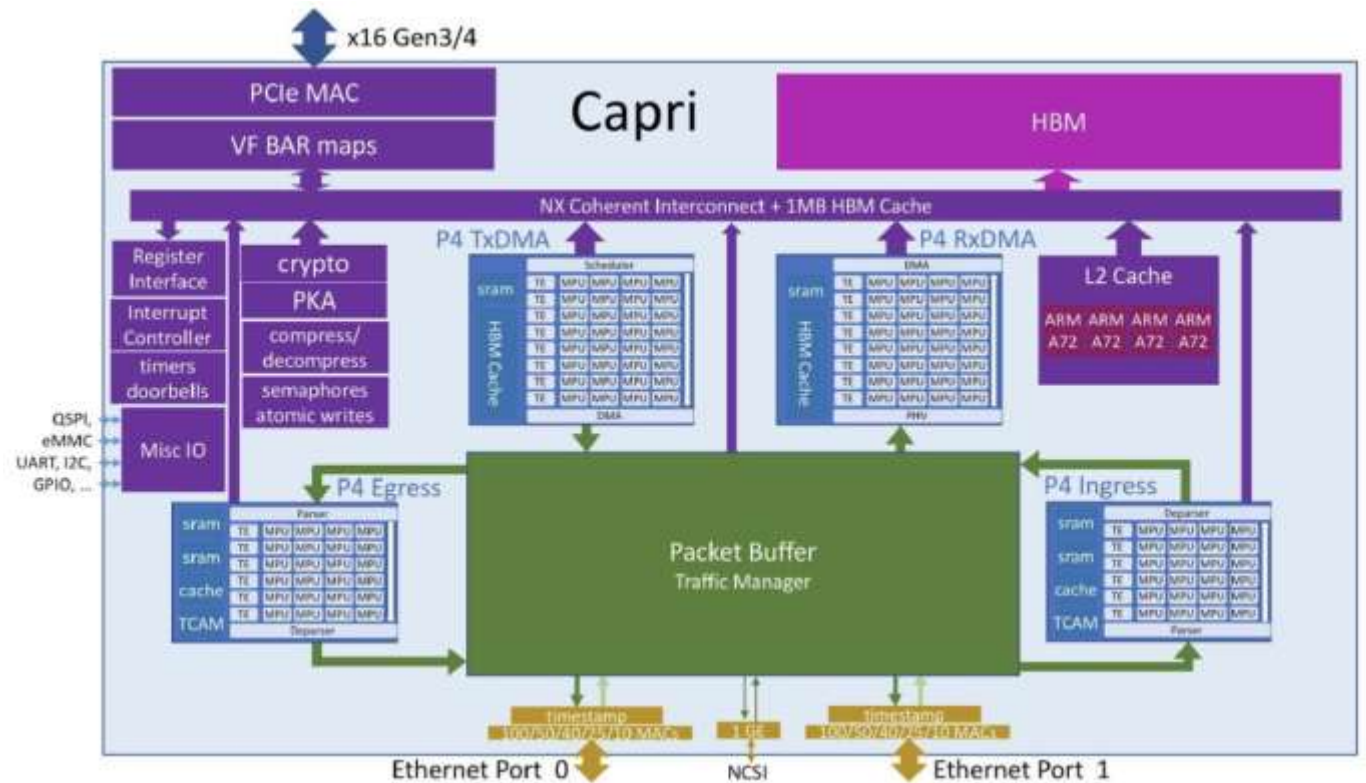
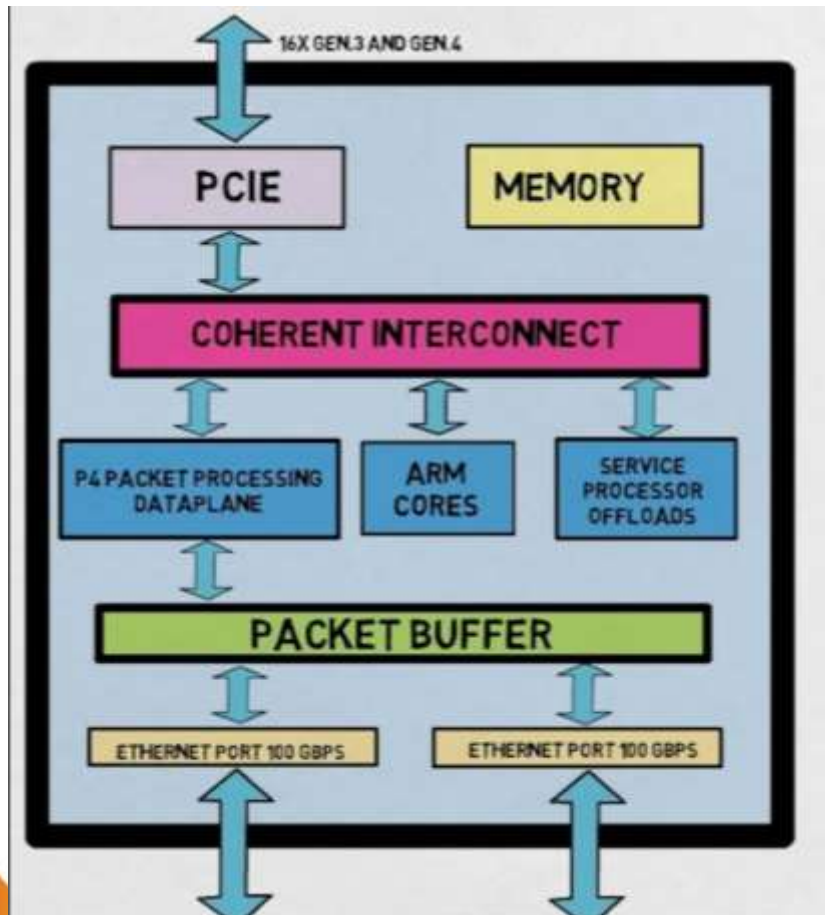
# Control vs. Data Plane



- Control Plane is the Coaching staff
  - Define & draw the plays
  - Select & deploy players
  - Orchestrate plays from the sidelines
  - 1/10GbE + Arm Complex
- Data Plane the Court, Players the Packet Engines
  - Move the ball
  - Execute the play
  - Listen to coaching staff
  - ASIC, Arm Complex and FPGA

# Architecture: Classic (Arms, IP & NoC)

## Pensando Oversimplified Capri





# Products: Classic

- Intel: Mt. Evans - 16x Arm Neoverse N1
- Fungible: MIPS cores, unique design, UDP acceleration
- NVIDIA:
  - BlueField 2 - 8xA72 Arm Cores —> \$1,500
  - BlueField 3 - 16xA78 Arm Cores, Fall 2022
- Pensando:
  - DSC25 P4 Engines & 4xA72 —> \$1,300
  - DSC100 (200) —> \$4,700



Pensando DSC-100 PCIe Card\*



# Products: Classic, Marvell

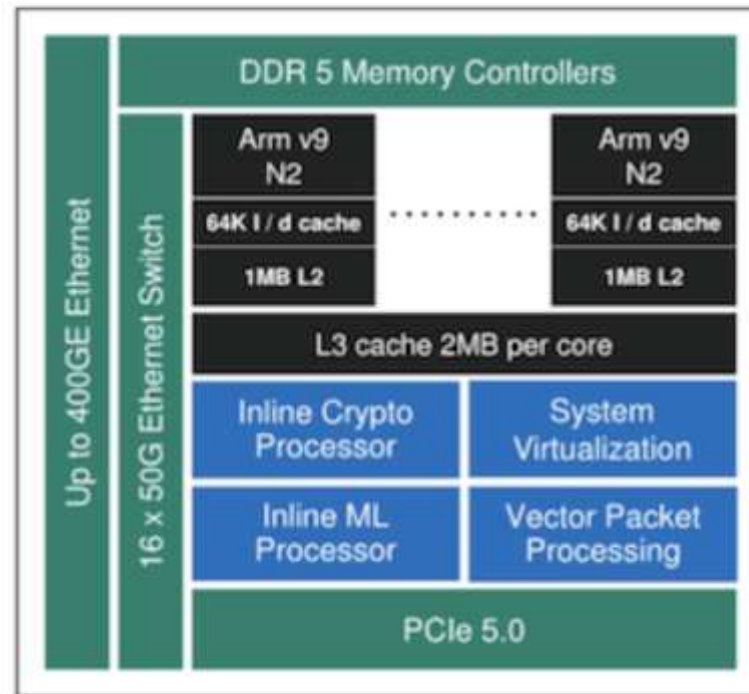
Four ASIC Family

8->36xNeoverse N2

25-60W

Chips Samples 6/21

## OCTEON 10 innovations



- 5nm TSMC process
  - Enables fanless designs
- First inline DPU ML Engine
- Hardware VPP acceleration
- Inline crypto processor
- Arm Neoverse N2 cores
  - Highest SPECint in industry
- PCIe 5.0, DDR5 support
- Integrated with 16x 50GE switch
- 56G SerDes

# Architecture: FPGA

High Tech Lego Style IP blocks

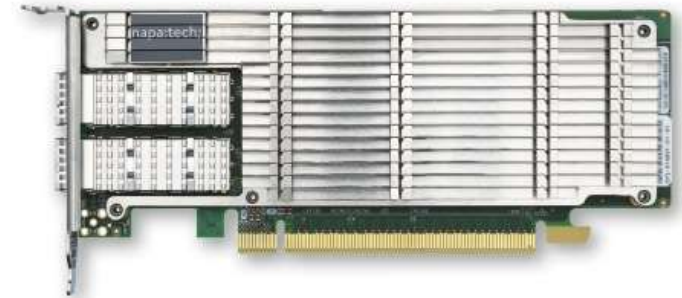
ASIC Logic Perimeter

Network on Chip (NoC)



# Products: FPGA

- Napatech
  - NT200A02, 2x100GbE, UltraScale+ VU5P
  - NT100A01, 4x25GbE, UltraScale+ VU5P
  - NT50B01, 2x25GbE, UltraScale+ VU5P



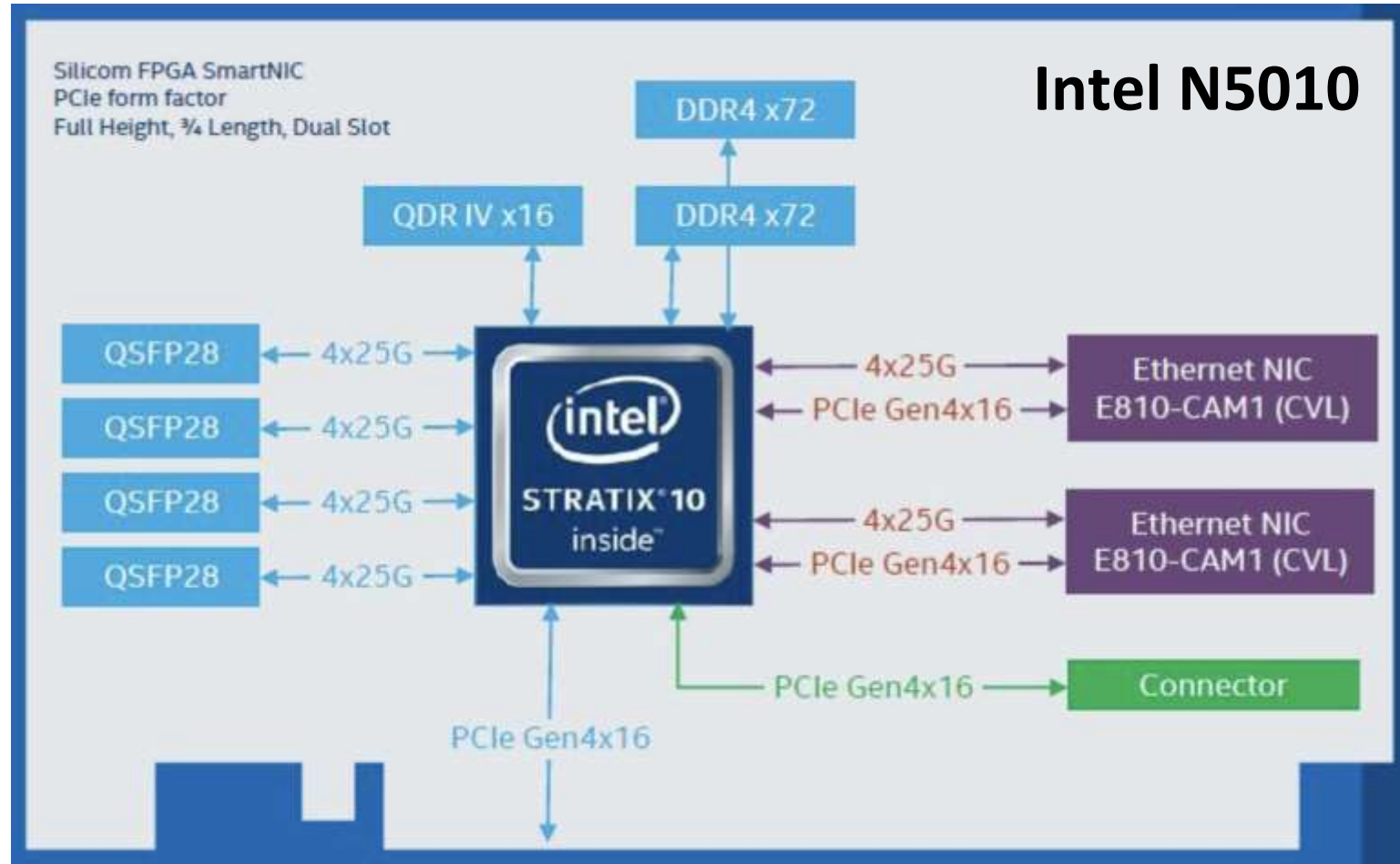
# Architecture: Hybrid

High Latency

3-Chip, expensive BoM

FPGA as Bump-in-wire

Programmable to a point





# Products: Hybrid

- AMD (Xilinx)
  - SN1022 (2x100G): Virtex, NXP 8xArm A72 —> \$2,400
  - U25 (2x25G): Zynq + X2 —> \$2,500
- Intel:
  - C5010X - FPGA/Xeon
  - N5010 - FPGA/2xE810



# Future Architectural Directions

- Control plane:
  - More powerful Arm/x86 Complex
  - Security concerns for physical separation, real out of band management
  - Growth of control plane OSeS
  - CXL expanded to enable greater SmartNIC control over host
- Data plane:
  - Explosion of Hard-IP
  - Chiplets will dominate in 2024 and beyond
  - Huge extensible FPGA fabrics supporting containerized bitstreams
  - More P4 Engines for increased traffic
  - More powerful ARM cores for complex packet transforms
  - AI/ML within FPGA fabric and chiplets may prove invaluable